

PATENT APPLICATION

Sheet 1 of 2

FORM PTO-1449		ATTY. DOCKET NO.	SERIAL NO.
		10001121-1	00/000,000
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT	U.S. PRO 09/908948
(Use several sheets if necessary)		Kenneth P. Park	07/19/01
		FILING DATE	GROUP
		Unknown	Unk

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1A					
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION	
							YES	NO
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>ED</i>	1Q	"A Logic Design Structure for LSI Testability", E.B. Eichelberger and T.W. Williams, Proc. 14th Design Automation Conf. IEEE Pub. 77CH1216-1C, June 1977, pp 462-468
<i>ED</i>	1R	"The Challenges of Design and Test for the World Wide Web", P. Gelsinger, Proc. International Test Conference, IEEE Pub. 99CH37034, Sept 1999, p 12
<i>ED</i>	1S	"Enhancing Testability of Large-Scale Integrated Circuits Via Test Points and Additional Logic", M.J.Y. Williams and J.B. Angell, IEEE Trans. on Computers, Jan 1973, vol C-22, no.1, pp 46-60

EXAMINER

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DATE CONSIDERED

08/22/06

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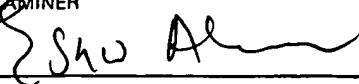
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
2A					
2B					
2C					
2D					
2E					
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2G					
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	2L							
	2M							
	2N							
	2O							
	2P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	"Design for Testability - A Survey", T.W. Williams and K.P. Parker, Proceedings of the IEEE, Jan. 1983, Vol 71, no. 1, pp 98-112
	2R	"The Boundary Scan Cell", Texas Instruments, JTAG IEEE 1149.1/P1149.4 Tutorial, Sept. 1997, Tut.I-20, Tut II-24-26
	2S	

EXAMINER 	DATE CONSIDERED 08/22/06
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